REMARKS

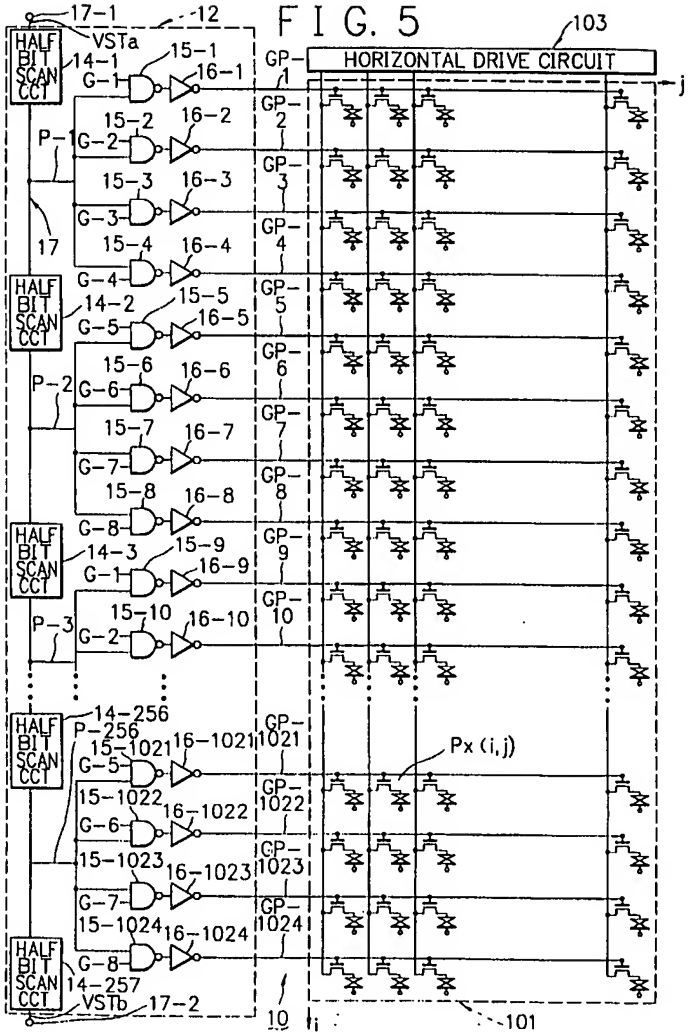
This amendment is in response to the Official Action dated July 13, 2007. Claims 1-4, and 9 have been amended, and claims 12-16 been added; as such claims 1-16 are currently pending in the application. Reconsideration and allowance of the pending claims is requested in consideration of the following remarks.

Claim Rejections under 35 USC § 102

Claims 1-11 remain rejected under 35 U.S.C. § 102(b) as being unpatentable over Asada et al. (U.S. Patent No. 5,883,609). Applicant respectfully traverses this rejection.

Asada teaches an implementation of an LCD capable of attaining multiple resolutions by adjusting the control signals used to drive the LCD. For example, Asada recognizes that a user may require an LCD to run at either a 1,024 x 1,280 resolution (1.0-fold), 480 x 680 resolution (2-fold), or a mid-range such as 800 x 600 (1.6-fold) (Asada at 1:59-2:6). The multi-resolution capability is achieved by identically driving control signals for adjacent scan lines (G-1 – G-8) (Asada at 15:14-32, 15:43-52, 16:13-29, and Figs. 5, 7, 8 and 23).

Fig 5 of Asada illustrates a vertical drive circuit 12 for driving the LCD display. Vertical drive circuit 12 produces a series of scan lines GP-1 to GP-1024. Each scan line is associated with a NAND gate 15-i and an inverter 16-i. Control signals (G-1 – G-8) selectively activate the individual scan lines making them only responsive to output signals (P-1 to P-n) (from the half-bit scan circuits) when a control signal G-i associated with the scan line is active.



(Fig 5 of Asada)

Figs. 7 and 8 illustrate timing diagrams for a sample 256 scanline display, and show the differences between control signals for driving the LCD at both a high (1-fold) and low (2-fold) resolution, respectively. In both Figs. 7 and 8 control signals drive the 256 (2^8) scan lines. A comparison of the driving diagrams shows that, in the 2-fold resolution of Fig. 8, adjacent pairs of control signals (G-1 - G-8) are driven identically at periods twice as long as in the 1-fold resolution setting in Fig. 7. By driving the control signals adjacent control signals are half the clock rate causes pairs of adjacent scan line to the same signals to the LCD, effectively reducing the resolution

of the display. Accordingly, Asada **does not modify the operation of the vertical drive circuit 12** in order to obtain lower resolutions, instead accomplishing the desired result using identical, adjacent control signals (Fig. 23).

Claim 1 recites: *[a] display device having at least a different resolution first mode and second mode having a lower resolution than said first mode, comprising:*

a pixel portion comprised of pixel circuits, for writing pixel data into pixel cells through switching elements, arranged so as to form a matrix of at least a plurality of rows;

a plurality of scan lines arranged so as to correspond to a row arrangement of said pixel circuits and controlling conduction of said switching elements;

at least one signal line arranged so as to correspond to a column arrangement of said pixel circuits and propagating said pixel data; and

a vertical drive circuit including a plurality of switch circuits, each switch circuit coupling an adjacent plurality of scan lines in the row direction, the switch circuits adapting the vertical drive circuit to

successively scan said scan lines in a row direction by scan pulses and successively select the pixel circuits connected to the scan lines in units of rows in said first mode, and

successively scan said scan lines for every adjacent plurality of scan lines in the row direction by the scan pulses and successively select the pixel circuits connected to said plurality of scan lines in units of the plurality of rows in said second mode.

Asada does not disclose, teach, or suggest "*...a vertical drive circuit including a plurality of switch circuits, each switch circuit coupling an adjacent plurality of scan lines in the row direction.*"

Asada includes a NAND gate, corresponding to each scan line, to control the output of the vertical drive circuit. **Each NAND gate controls the output of a single scan line.** By adjusting the

control signals (G-1 to G-8) independently (as illustrate in Asada Figure 7 and 8), the Asada system groups the output of certain adjacent scan lines using synchronized control signals.

Asada does not teach or suggest using a single switch (or NAND gate) to control a plurality of scan lines. Instead, , as illustrated in Figure 5 of Asada (provided above), Asada teaches that each NAND gate accepts an input control signal which operates the NAND gate independently. Furthermore, each NAND gate only affects a single scan line.

By contrast, claim 1 is directed to a plurality of switch circuits, where "***each*** *switch circuit coupling an adjacent* ***plurality*** *of scan lines*."

Furthermore, Asada not only does not teach the claimed invention, but also effectively teaches away from it, by providing a **completely distinct alternative** means of reducing screen resolution.

Accordingly, Asada fails to disclose, teach or suggest the features of independent claim 1. For similar reasons, independent claim 9 is also neither disclosed nor suggested by Asada (although claims 1 and 9 should be interpreted solely based upon the limitations set forth therein). Therefore, Applicant respectfully requests that the rejection of independent claims 1 and 9 and dependent claims 2-8 and 10-11 under 35 U.S.C. § 102(b) be withdrawn.

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 18-0013, under Order No. SON-2919 from which the undersigned is authorized to draw.

Dated: October 15, 2007

Respectfully submitted,

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Attachments: Amendment Transmittal

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